Amendments to the Specification:

Please replace the paragraphs with the following amended paragraphs:

[0004] In general, as shown in Figure 1B, a matched number of metal layers 122 are situated on either side of a core material 126, a thicker "backbone" layer typically comprised of the material used in the dielectric layers 124. A balanced number of metal layers 122 on either side of the core 126 contributes to less substrate warpage resulting from uneven expansion of the various substrate layers 122 and 124 when heated. Photo-definable solder mask layers 128 typically protect the top and bottom metal layers 122 of the substrate. For clarity, the topmost solder mask layer 128 is not shown in Figure 1A. A photolithography process is typically used to create openings in areas of the solder mask layers 128, exposing the appropriate underlying area of metal layer [[128]] 122 for interconnection.

[0005] In the exemplary configuration shown in Figure 1B, the substrate 120 has four metal layers 122, and is consequently called a "four-layer" substrate. Typically, the first metal layer (or [[n]] the n^{th} metal layer) 140, as counted from the substrate top, is a signal layer, to which the signals and other addresses on the die 110 are wirebonded or otherwise coupled. The die 110 is shown interconnected to the signal layer 140 with bond wires 152. Layers 142, 144 and 146 typically comprise a ground plane, power plane and ball layer, respectively. Ground plane 142 and power plane 146 often include relatively sturdy planes, or large patterns of metal less susceptible to damage than relatively narrow traces 160. Die bond pads 154 assigned to power or ground are interconnected with the power plane 142 or ground plane 146, respectively, by vias 162, cylindrical columns of conductive material for interconnecting two metal layers 122. It will be understood that power and ground metal may share the same metal layer 122, each having a unique area of metal electrically insulated from the other by an interstitial dielectric 150 or other insulating material. The ball layer metal 146 is typically

configured into conductive areas, or lands 170, each attached to a solder ball 164, which may be later reflowed to a PCB, interconnecting the die 110 to the PCB.

[0010] Figure 2 is a partial cross-sectional view of a simplified version of Figure 1B, with like parts having like reference numerals. As shown in Figure 1B, in a typical configuration, top metal layer, or [[*n*]] *n^th^* metal layer 140, includes a signal metal layer. The second metal layer, or *n-1* layer 142, as counted from the top includes a ground plane. The third metal layer, or *n-2* layer 144, includes a power plane. The fourth metal layer, or *n-3* layer 146, includes a land metal plane, which may include "lands," or conductive areas with which an interconnector (e.g., a solder ball or spring) may be contacted to produce electrical interconnection with a PCB.

[0011] As previously discussed, disposing a signal metal layer on the *n* metal layer may subject relatively fragile signal traces to excessive mechanical stresses. Generally, the further a component is away from an interface with a large CTE mismatch, the less mechanical stresses are incident on the component from the CTE mismatch. It is therefore desired to design a substrate such that mechanical stress impact is lessened to the critical signal traces with minimal impact to other metal layers. Figure 3 shows a simplified view of a partial cross-section of a recessed-bond semiconductor package substrate 320 in accordance with a preferred embodiment. A top metal layer, or [[n]] n^th^ metal layer 340, preferably includes a ground plane. A second metal layer, or *n-1* layer 342, as counted from the top, preferably includes a signal layer. While the top metal layer is denoted as the [[*n*]] n^th^ layer, a subsequent (or underlying) metal layer is denoted as an *n-k* layer, where *k* represents the number of metal layers a particular metal layer is removed from the [[*n*]] n^th^ layer. It will be understood that this nomenclature is independent of the total number of metal layers within a substrate. A third metal layer, or *n-2* layer 344, preferably includes a power plane, and a fourth metal layer, or *n-3* layer 346, preferably includes a land plane. "Lands" are conductive areas with which an interconnector (e.g., a solder ball or spring) may be contacted to produce

electrical interconnection with a PCB. Disposing the signal layer on the *n-1* metal layer 342 adds physical support to the relatively fragile signal traces. Instead of being disposed on the outermost (i.e., [[*n*]] $\underline{n^{th}}$ n metal) layer 340, in the preferred embodiment, the signal layer is layered underneath at least one metal layer, shielding it from higher CTE-mismatch forces possible within the *n* metal layer.

[0017] Figure 3 shows a simplified view of a partial cross-section of a recessed-bond semiconductor package substrate 320 in accordance with a preferred embodiment. A top metal layer, or [[*n*]] $\underline{n^{th}}$ metal layer 340, preferably includes a ground plane. A second metal layer, or *n-1* layer 342, as counted from the top, preferably includes a signal layer. While the top metal layer is denoted as the [[*n*]] $\underline{n^{th}}$ layer, a subsequent (or underlying) metal layer is denoted as an *n-k* layer, where *k* represents the number of metal layers a particular metal layer is removed from the [[*n*]] $\underline{n^{th}}$ layer. It will be understood that this nomenclature is independent of the total number of metal layers within a substrate. A third metal layer, or *n-2* layer 344, preferably includes a power plane, and a fourth metal layer, or *n-3* layer 346, preferably includes a land plane. "Lands" are conductive areas with which an interconnector (e.g., a solder ball or spring) may be contacted to produce electrical interconnection with a PCB. Disposing the signal layer on the *n-1* metal layer 342 adds physical support to the relatively fragile signal traces. Instead of being disposed on the outermost (i.e., [[*n*]] $\underline{n^{th}}$ metal) layer 340, in the preferred embodiment, the signal layer is layered underneath at least one metal layer, shielding it from higher CTE-mismatch forces possible within the [[*n*]] $\underline{n^{th}}$ metal layer.

[0018] It will be understood that orientation comments relating to the position of the metal layers within the package substrate are with respect to the die mounted on the substrate. For example, referencing an *n-1* layer as located "below" an [[*n*]] $\underline{n^{th}}$ metal layer will indicate that the *n-1* layer is disposed farther removed from the die than is the

[[*n*]] nth metal layer. The top metal layer of a substrate, or closest metal layer to the die is the [[*n*]] nth metal layer, with each underlying layer denoted as *n-1, n-2, n-3,* etc.

[0019] Figure 4 shows a more detailed view of the substrate 320 shown in Figure 3, configured with a semiconductor package assembly 400. Instead of positioning the signal metal 402 on the [[*n*]] nth metal layer 440, as with conventional substrate designs, the signal layer is positioned below the [[*n*]] nth metal layer within the substrate. Bond wires 452 pass through a substrate bond opening 404 in the solder mask layer 428, [[*n*]] nth metal layer 440, and a first dielectric layer 424 to connect the signal metal 402 disposed on the *n-1* metal layer 442 to an integrated circuit, or semiconductor, die 410. The recessed-bond substrate is so named because the metal layer to which the die is directly interconnected is recessed below the top metal layer 440. The substrate bond openings 404 in the solder mask layer 428, [[*n*]] nth metal layer 440, and the dielectric layer 424 may be created using any method known in the art, including photolithography and etching processes. It will be understood that, while the preferred embodiment shown in Figure 4 illustrates a signal layer 402 disposed on the *n-1* layer 442, the signal layer may be disposed on a subsequent metal layer 422 (e.g., *n-2* layer 444, *n-3* layer 446).

[0021] In a typical configuration, a semiconductor package assembly may heat up during operation. The various materials may consequently expand at differing rates. In particular, a more expansive substrate dielectric material (e.g., bismaleimide triazine (BT) with a CTE of about 50 ppm/C), may stretch the less expansive metal layers (e.g., copper with a CTE of about 17 ppm/C) within a substrate. This CTE mismatch may apply particular stress on the metal layer closest to the die (i.e., the [[*n*]] nth metal layer). In turn, the upper layers of the substrate are somewhat restricted from expanding by their attachment to the low-CTE die (e.g., silicon with a CTE of about 3 ppm/C), resulting in relatively high stresses in the die.

[0023] In the preferred embodiment shown in Figure 4, the signal layer metal 402 is disposed on the *n-1* layer 442 and shielded from the die 410 by a dielectric layer 424, a metal layer (e.g., a ground plane) 440, and the solder mask layer 428. By allowing the placement of a larger plane of metal (e.g., a copper ground plane with a CTE of about 17 ppm/C) within the [[*n*]] $\underline{n^{th}}$ metal layer 440, the preferred embodiment lowers the effective CTE of this layer by reducing the amount of interstitial substrate material (e.g., BT with a CTE of about 50 ppm/C) present in the layer. Increasing the metal and decreasing the amount of substrate dielectric material within the layer brings the [[*n*]] $\underline{n^{th}}$ metal layer 440 more in line with the CTE of the adjacent silicon die 410, which generally has a CTE of about 3 ppm/C. The possibility of lowering the effective CTE of the [[*n*]] $\underline{n^{th}}$ metal layer 440 decreases the likelihood of delamination at the die-substrate interface 406.

[0025] Electrical benefits can also be obtained by placing the signal layer metal 402 below the [[*n*]] $\underline{n^{th}}$ metal layer 440 of the substrate 320. When electrical signals propagate with different velocities at various frequencies, the result is called dispersion. Dispersion is generally a result of different electromagnetic field configurations, which may result from the different frequencies involved in a signal. For a typical high-speed signal with a rise time of about 35 picoseconds (ps), the frequency content of the digital pulse may be about 20 Gigahertz (GHz). Dispersion may likely cause the rise time and system noise to increase. Rise time is typically defined as the time required for a signal to change from a specified low value to a specified high value. Faster rise times contribute to faster electronic devices, and as such, reducing rise times is generally desired. System noise may be defined as a disturbance that affects a signal and that may distort the information carried by a signal. Keeping system noise to a minimum is also desired.

[0028] Disposing a ground plane on the [[*n*]] $\underline{n^{th}}$ metal layer 440 may reduce the radiation emanating from the package by reducing the overall length of the signal path

that is open to radiation to the length of the bond wire 452. As the majority of the signal metal 402 on *n-1* layer 442 may be shielded by the overlying [[*n*]] $\underline{n^{th}}$ metal layer 440, less radiation may be able to propagate from the signal metal. Radiation efficiency from the edge of a plane, such as the edge of *n-1* layer 442 exposed on the outer edge of substrate 320, is much less than that from an exposed printed circuit trace. By reducing the overall length of the exposed trace to that of the bond wire 452 alone, the radiation is reduced by a factor proportional to the square of the length of the exposed trace.

[0029] Disposing a ground plane on the [[*n*]] $\underline{n^{th}}$ metal layer 440 may also offer the possibility of eliminating vias to the top surface of the substrate 320. Referring briefly back to Figure 1B, in a typical configuration, the bond wires 152 are bonded directly to the top, [[*n*]] $\underline{n^{th}}$ metal layer 140 and must follow via 162 to the *n-1* layer 142. As shown in Figure 4, in a substrate in accordance with the preferred embodiments, bond wires 452 are bonded directly to the *n-1* layer 442, eliminating the need for a via to reach this layer. The elimination of this layer of vias may contribute to significant package cost savings while still allowing good routability. Eliminating vias from the [[*n*]] $\underline{n^{th}}$ metal layer 440 to the signal metal 402 may contribute to a "clean" ground plane 440, meaning that via holes would not need to be created through the ground metal, interrupting the plane. A clean ground plane may be electrically preferable for high-speed signal traces, with which a well-defined ground-plane current path is desired.

[0031] As the signal metal 402 in the preferred embodiments is not disposed directly under the die 410 on the [[*n*]] $\underline{n^{th}}$ metal layer 440, greater routing flexibility can be achieved. Referring briefly back to Figure 1B, in conventional substrate designs, bond wires 152 attach to substrate bond pads 156, from which signal traces 160 route out towards the perimeter of the substrate 120. This configuration may be acceptable for lower pin-count substrates, but as semiconductor dies increase in complexity, the need rises to package dies with ever-increasing pin-counts into smaller packages. Unlike the "depopulated-array" substrate 120 shown in Figure 1B, in which solder balls 164 are

only located on the substrate periphery, many substrates are designed as "full array" substrates. In full-array substrates, an array of solder balls is distributed over the entire area of the substrate.

[0032] Routing a die to solder balls on full-array substrates is often a challenge. Compounding this challenge is the fact that many of today's semiconductor package assemblies utilize chip-scale package (CSP) technology, in which the die has nearly the same area as the package substrate. To reach inner balls, the need may exist to route signals under the footprint of the die itself. In a conventional substrate, this may require routing signal traces immediately underneath the die on the [[*n*]] $\underline{n^{th}}$ metal layer, an area of particularly high stress. A package substrate in accordance with the preferred embodiments reduces the risk associated with routing the signal layer immediately under the die footprint, by the placement of the signal layer on the *n-1* layer or below.